AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 25, 28, 31 and 34 as follows:

LISTING OF CLAIMS:

1. – 24. (Cancelled).

25. (Currently Amended) A semiconductor device comprising:

an active area with at least one MOS transistor to be formed therein;

an insulation film for defining said active area, said insulation film having a top surface; and

a current/leakage prevention portion for preventing current leakage,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third

edge, said fourth edge extending in a direction opposite from said second edge, and said active area having a fifth edge connected to a second end opposite from said first end of second edge, said fifth edge being parallel to said third edge and said fifth edge extending in a direction opposite from said first edge,

said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, and said first and second gate electrodes being parallel to one another and ~~disposed directly adjacent to each other~~ having a source/drain disposed therebetween,

said current/leakage prevention portion including

a first end of said first gate electrode extending beyond said fourth edge and extending over the top surface of said insulation film,

a first end of said second gate electrode extending beyond said third edge and extending over the top surface of said insulation film, and

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said

third edge to said first end thereof, the second length of said second gate electrode being greater than the first length of said first gate electrode and the second length having a first portion extending between the third edge to a virtual line of said fifth edge extended in a horizontal direction and a second portion of the second length of said second gate electrode, extending beyond the virtual line of said fifth edge to said first end thereof, the second portion being equal in length to said first length of said first gate electrode.

26. (Previously Presented) The semiconductor device according to claim 25, wherein

said first edge is greater in length than said second edge, and

said second length is greater than at least the length of said second edge.

27. (Previously Presented) The semiconductor device according to claim 26, wherein

said second length is a sum of said first length and the length of said second edge.

28. (Currently Amended) [[The]] A semiconductor device ~~according to claim 26~~ comprising:

an active area with at least one MOS transistor to be formed therein;

an insulation film for defining said active area, said insulation film having a top surface; and

a current/leakage prevention portion for preventing current leakage,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, and said first and second gate electrodes being parallel to one another and having a source/drain disposed therebetween,

said current/leakage prevention portion including

a first end of said first gate electrode extending beyond said fourth edge and extending over the top surface of said insulation film,

a first end of said second gate electrode extending beyond said third edge and extending over the top surface of said insulation film, and

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the second length of said second gate electrode being greater than the first length of said first gate electrode, wherein

said second length is a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

29. (Previously Presented) The semiconductor device according to claim 25, wherein

said second length is greater than the lengths of said first and second edges.

30. (Previously Presented) The semiconductor device according to claim 29, wherein

said first and second gate electrodes are parallel to each other, and

said first end of said first gate electrode and said first end of said second gate electrode are in a line.

31. (Currently Amended) A method of manufacturing a semiconductor device including an active area with at least one MOS transistor to be formed therein, and an insulation film for defining said active area, based on layout design comprising the steps of:

(a) configuring said active area to have a recess in plan configuration; and

(b) configuring a first MOS transistor having a first gate electrode and a second MOS transistor having a second gate electrode on said active area, and configuring said first and second gate electrodes to be parallel to one another and having a source/drain region disposed ~~directly adjacent to each other~~ therebetween,

said step (a) including the steps of

configuring said recess to be defined by first, second and third edges, said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and a first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend, [[and]]

configuring a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge, and

configuring a fifth edge connected to a second end opposite from said first end of said second edge, said fifth edge being parallel to said third edge, said fifth edge extending in a direction opposite from said first edge,

said step (b) including the steps of

configuring said first gate electrode to extend in a direction perpendicular to the direction in which said fourth edge extends, and

configuring said second gate electrode to extend in a direction perpendicular to the direction in which said third edge extends, and

configuring a current/leakage prevention portion to prevent current leakage by configuring said first gate electrode to have a first end extend beyond said fourth edge and extend over a top surface of said insulation film and configuring said second gate electrode to have a first end extend beyond said third edge and extend over the top surface of said insulation film, said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the second

length of said second gate electrode being greater than the first length of said first gate electrode, and the second length having first and second portions, the first portion extending between the third edge and a virtual line of the fifth edge extended in a horizontal direction, the second portion extending beyond the virtual line of the fifth edge to the first end thereof, the second portion being equal in length to the first length of the first gate electrode.

32. (Previously Presented) The method according to claim 31, wherein

said step (a) includes configuring said first edge to be greater in length than said second edge, and

said step (b) includes configuring said second length to be greater than at least the length of said second edge.

33. (Previously Presented) The method according to claim 32, wherein

said step (b) includes configuring said second length to equal a sum of said first length and the length of said second edge.

34. (Previously Presented) [[The]] A method ~~according to claim 32~~ of manufacturing a semiconductor device including an active area with at least one MOS transistor to be formed therein, and an insulation film for defining said active area, based on layout design comprising the steps of:

(a) configuring said active area to have a recess in plan configuration; and

(b) configuring a first MOS transistor having a first gate electrode and a second MOS transistor having a second gate electrode on said active area, and configuring said first and second gate electrodes to be parallel to one another and having a source/drain region disposed therebetween,

said step (a) including the steps of

configuring said recess to be defined by first, second and third edges, said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and a first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend, and

configuring a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said step (b) including the steps of

configuring said first gate electrode to extend in a direction perpendicular to the direction in which said fourth edge extends, and

configuring said second gate electrode to extend in a direction perpendicular to the direction in which said third edge extends, and

configuring a current/leakage prevention portion to prevent current leakage by configuring said first gate electrode to have a first end extend beyond said fourth edge and extend over a top surface of said insulation film and configuring said second gate electrode to have a first end extend beyond said third edge and extend over the top surface of said insulation film, said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the second length of said second gate electrode being greater than the first length of said first gate electrode, wherein

said step (b) includes configuring said second length to equal a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

35. (Previously Presented) The method according to claim 31, wherein

said step (b) includes configuring said second length to be greater than the lengths of said first and second edges.

36. (Previously Presented) The method according to claim 35, wherein

said step (b) includes

configuring said first end of said first gate electrode and said first end of said second gate electrode to be in a line.